Amendments to the Claims:

Claim 1 (Currently amended): A method of forming a dual damascene structure, wherein a substrate ~~least one wire on a substrate, the substrate~~ comprising at least one conductive region is provided, wherein the conductive region is utilized as a first alignment mark, an insulating layer disposed on the substrate, the method comprising:

forming a hard mask layer on a surface of the insulating layer;

forming at least one via and one recess by removing portions of the hard mask layer and portions of the insulating layer;

forming a light blocking layer on a surface of the hard mask layer and the recess, the light blocking layer and the hard mask layer forming a composite layer;

forming a gap filling layer on a surface of the light blocking layer, and the gap filling layer filling up the recess;

forming a photoresist layer on a surface of the gap filling layer;

aligning a photo mask with the recess by utilizing the composite layer as a mask, wherein the recess is utilized as a second alignment mark, and light is prevented from reaching to the first alignment mark by the composite layer when aligning the photo mask with the second alignment mark to achieve two direct alignments; ~~and~~

performing an exposure and development process to form at least one pattern above the recess in the photoresist layer~~.~~; and

performing an etching process for forming a trench directly on the via.

Claim 2 (Original): The method of claim 1 wherein the substrate comprises a semiconductor wafer or a silicon-on-insulator substrate (SOI substrate).

Claim 3 (Original): The method of claim 1 wherein the conductive region comprises a source of a transistor, a gate of a transistor, a drain of a transistor, a lower level wire, a landing pad, or a resistor, and the recess is formed above the conductive region.

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Claim 4 (Cancelled)

Claim 5 (Currently amended): The method of claim 41, wherein the formation of the trench further comprises ~~further comprising the following steps after forming the pattern in the photoresist layer~~:

performing an etching process by utilizing the photoresist layer as a mask to remove portions of the gap filling layer, the light blocking layer, the hard mask layer, and the insulating layer to form at least one trench of at least one dual damascene structure;

removing the photoresist layer;

removing the remaining gap filling layer;

forming a barrier layer on a surface of the light blocking layer and the dual damascene structure;

performing a re-sputter process to expose the conductive region;

forming a seed layer on a surface of the barrier layer and the exposed conductive layer; and

forming a metal layer on a surface of the seed layer, and the metal layer filling up the dual damascene structure.

Claim 6 (Cancelled)

Claim 7 (Cancelled)

Claim 8 (Original): The method of claim 1 wherein the conductive region is the first alignment mark, and the recess is formed aside the conductive region.

Claim 9 (Original): The method of claim 8 wherein the composite layer is used to prevent light from reaching to the conductive region when aligning the photo mask with the recess to improve alignment accuracy.

Claim 10 (Original): The method of claim 1 wherein the hard mask layer is a titanium nitride layer (TiN layer).

Claim 11 (Original): The method of claim 10 wherein a thickness of the titanium nitride layer is approximately 250 angstroms (Å).

Claim 12 (Original): The method of claim 1 wherein the light blocking layer comprises a titanium nitride layer or a tantalum nitride layer (TaN layer).

Claim 13 (Original): The method of claim 12 wherein a thickness of the titanium nitride layer is approximately 250 angstroms (Å).

Claim 14 (Original): The method of claim 1 wherein the gap filling layer is a bottom anti-reflective coating (BARC) and is formed by a spin coating process.

Claim 15 (Currently amended): A method of forming a dual damascene structure, wherein a substrate ~~at least one wire on a substrate, the substrate~~ comprising at least one ~~first~~ conductive region is provided ~~and at least one second conductive region~~, wherein the ~~second~~ conductive region is utilized as a first alignment mark, an insulating layer disposed on the substrate, the method comprising:

forming a hard mask layer on a surface of the insulating layer;

forming at least one trench and one ~~first~~ recess above the first conductive region and at least one recess aside the second conductive region by removing portions of the hard mask layer and portions of the insulating layer;

forming a light blocking layer on a surface of the hard mask layer~~,~~ and the ~~first~~ recess, ~~and the second recess,~~ the light blocking layer and the hard mask layer forming a composite layer;

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forming a gap filling layer on a surface of the light blocking layer, and the gap filling layer filling up the ~~first~~ recess ~~and the second recess~~;

forming a photoresist layer on a surface of the gap filling layer;

aligning a photo mask with the ~~second~~ recess by utilizing the composite layer as a mask, wherein the ~~second~~ recess is utilized as a second alignment mark, and light is prevented from reaching to the first alignment mark by the composite layer when aligning the photo mask with the second alignment mark to achieve two direct alignments; ~~and~~

performing an exposure and development process to form at least one pattern above the first recess in the photoresist layer~~.~~; and

performing an etching process for forming a via directly on the trench.

Claim 16 (Original): The method of claim 15 wherein the substrate comprises a semiconductor wafer or a silicon-on-insulator substrate (SOI substrate).

Claim 17 (Original): The method of claim 15 wherein the first conductive region comprises a source of a transistor, a gate of a transistor, a drain of a transistor, a lower level wire, a landing pad, or a resistor.

Claim 18 (Cancelled)

Claim 19 (Cancelled)

Claim 20 (Cancelled)

Claim 21 (Currently amended): The method of claim ~~20~~15, wherein the formation of the via further comprises ~~further comprising the following steps after forming the pattern in the photoresist layer~~:

performing an etching process by utilizing the photoresist layer as a mask to

remove portions of the gap filling layer, the light blocking layer, the hard mask layer, and the insulating layer to form at least one via of at least one dual damascene structure;

removing the photoresist layer;

removing the remaining gap filling layer;

forming a barrier layer on a surface of the light blocking layer and the dual damascene structure;

performing a re-sputter process to expose the first conductive region;

forming a seed layer on a surface of the barrier layer and the exposed first conductive region; and

forming a metal layer on a surface of the seed layer, and the metal layer filling up the a dual damascene structure.

Claim 22 (Cancelled)

Claim 23 (Original): The method of claim 15 wherein the hard mask layer is a titanium nitride layer (TiN layer).

Claim 24 (Original): The method of claim 23 wherein a thickness of the titanium nitride layer is approximately 250 angstroms (Å).

Claim 25 (Original): The method of claim 15 wherein the light blocking layer comprises a titanium nitride layer or a tantalum nitride layer (TaN layer).

Claim 26 (Original): The method of claim 25 wherein a thickness of the titanium nitride layer is approximately 250 angstroms (Å).

Claim 27 (Original): The method of claim 15 wherein the gap filling layer is a bottom anti-reflective coating (BARC) and is formed by a spin coating process.

Claim 28 (Original): A method of forming at least one wire on a substrate, the substrate comprising at least one first conductive region and at least one second conductive region, wherein the second conductive region is utilized as a first alignment mark, an insulating layer disposed on the substrate, the method comprising:

forming at least one first recess above the first conductive region and at least one recess aside the second conductive region by removing portions of the insulating layer;

forming a bottom anti-reflective coating (BARC) on a surface of the insulating layer, the first recess, and the second recess, and the bottom anti-reflective coating filling up the first recess;

forming a photoresist layer on a surface of the bottom anti-reflective coating, and the photoresist layer filling up the second recess;

aligning a photo mask with the second recess by utilizing the bottom anti-reflective coating as a mask, wherein the second recess is utilized as a second alignment mark, and light is prevented from reaching to the first alignment mark when aligning the photo mask with the second alignment mark to achieve two direct alignments; and

performing an exposure and development process to form at least one pattern above the first recess in the photoresist layer.

Claim 29 (Original): The method of claim 28 wherein the substrate comprises a semiconductor wafer or a silicon-on-insulator substrate (SOI substrate).

Claim 30 (Original): The method of claim 28 wherein the first conductive region comprises a source of a transistor, a gate of a transistor, a drain of a transistor, a lower level wire, a landing pad, or a resistor.

Claim 31 (Original): The method of claim 30 wherein the first recess exposes the first conductive region.

Claim 32 (Original): The method of claim 31 further comprising the following steps after forming the pattern in the photoresist layer:

performing an etching process by utilizing the photoresist layer as a mask to remove portions of the bottom anti-reflective coating and the insulating layer to form at least one trench of at least one dual damascene structure;

removing the photoresist layer;

removing the remaining bottom anti-reflective coating;

forming a barrier layer on a surface of the insulating layer and the dual damascene structure;

performing a re-sputter process to expose the first conductive region;

forming a seed layer on a surface of the barrier layer and the exposed first conductive region; and

forming a metal layer on a surface of the seed layer, and the metal layer filling up the dual damascene structure.

Claim 33 (Original): The method of claim 30 wherein the recess does not expose the first conductive region.

Claim 34 (Original): The method of claim 33 further comprising the following steps after forming the pattern in the photoresist layer:

performing an etching process by utilizing the photoresist layer as a mask to remove portions of the bottom anti-reflective coating and the insulating layer to form at least one via of at least one dual damascene structure;

removing the photoresist layer;

removing the remaining bottom anti-reflective coating;

forming a barrier layer on a surface of the insulating layer and the dual damascene structure;

performing a re-sputter process to expose the first conductive region;

forming a seed layer on a surface of the barrier layer and the exposed first conductive region; and

forming a metal layer on a surface of the seed layer, and the metal layer filling up the a dual damascene structure.

Claim 35 (Original): The method of claim 28 wherein the second conductive region is the second alignment mark, and the bottom anti-reflective coating is used to prevent light from reaching to the second conductive region when aligning the photo mask with the second recess to improve alignment accuracy.

Claim 36 (Original): The method of claim 28 wherein the bottom anti-reflective coating is a light absorptive coating.

Claim 37 (Original): The method of claim 28 wherein a thickness of the bottom anti-reflective coating is approximately 600~1200 angstroms (Å).

Claim 38 (Original): The method of claim 28 wherein the bottom anti-reflective coating is composed of organic materials, and the bottom anti-reflective coating is formed by a spin coating process.

Claim 39 (Original): The method of claim 38 wherein the organic materials comprises dyes.